above-mentioned heavily-doped regions, are formed, and then metal lines connected to the contacts **123**, **129**, **135**, **141**, and **187** are formed. As such, the semiconductor device **100** according to the embodiments of the present disclosure is formed.

[0040] In the embodiments, the first lightly-doped region **150** and the third high voltage lightly-doped region **131** are formed in the same manufacturing process, such that these two regions may diffuse and expand simultaneously in the following thermal process, and the first lightly-doped region **150** can prevent the third high voltage lightly-doped region **131** from expanding too much causing punch through between the lightly-doped region **131** and the heavily-doped region **121**.

[0041] In an embodiment, an operating method of the semiconductor device according to the embodiments of the present disclosure is provided. Referring to FIGS. **1**A-**1**B, in addition to the contacts **123**, **135**, **141**, and **187** respectively connected to the source region **120**, the drain region **130**, the gate structure **140**, and the doped ring structure **180**, the individual connecting pin **171** of the second isolation region **170** can receive an individual voltage, which is applied independently from other voltages applied to the source region **120**, the drain region **130**, the gate structure **140**, and the doped ring structure **180**. As such, the semiconductor device of the present disclosure can be operated in two different modes.

[0042] When the voltage Vd applied to the drain region **130** is equal to the voltage Viso-d applied to the second isolation region **170**, and the source region **120** and the doped region (doped ring structure **180**) are grounded, a positive voltage can be applied to the gate structure **140**. In such case, the semiconductor device performs a positive voltage operation.

[0043] When the voltage Vd applied to the drain region **130** is different from the voltage Viso-d applied to the second isolation region **170**, the source region **120** has a negative voltage, and the doped region (doped ring structure **180**) is grounded, a negative voltage can be applied to the gate structure **140**. In such case, the semiconductor device performs a negative voltage operation.

[0044] FIGS. **3**A-**3**B show I-V curves of a semiconductor device according to the embodiments of the present disclosure under positive voltage operations and negative voltage operations, respectively. As shown in FIG. **3**A, in the embodiment, while the voltage Vd applied to the drain region **130** and the voltage Viso-d applied to the second isolation region **170** are equipotential, the semiconductor device can perform a positive voltage operation, and the I-V curves are nicely shown in FIG. **3**A. In the positive voltage operation mode, the voltage Vg applied to the gate structure **140** is about 1V to 5V, and the drain voltage Vd is about 0 to 33 V. As shown in FIG. **3**B, in the embodiment, while the voltage Vd applied to the drain region **130** is different from the voltage Viso-d applied to the second isolation region **170**, the semiconductor device can perform a negative voltage operation, and the I-V curves are nicely shown in FIG. **3**B. In the negative voltage operation mode, the voltage Vg applied to the gate structure **140** is about −7 V to −11 V, the drain voltage Vd is about −12 V to 12 V, the voltage Viso-d applied to the second isolation region **170** is about 12 V, and the negative voltage Vs of the source region **120** is about −12 V.

[0045] In summary, the second isolation region **170** can receive an individual voltage, which is applied independently from other voltages applied to the other regions; therefore, the semiconductor device according to the embodiments of the present disclose can perform a positive voltage operation and a negative voltage operation.

[0046] While the invention has been described by way of example and in terms of the preferred embodiment(s), it is to be understood that the invention is not limited thereto. On the contrary, it is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

What is claimed is:

1. A semiconductor device, comprising:
- a substrate;
- a source region and a drain region formed in the substrate;
- a gate structure formed on the substrate and between the source region and the drain region;
- a first lightly-doped region formed below the source region; and
- a first isolation region formed in the substrate and surrounding the source region, the drain region, and the first lightly-doped region;
- wherein the source region and the drain region have a first-polarity, and the first lightly-doped region and the first isolation region have a second-polarity.

2. The semiconductor device according to claim **1**, wherein the first-polarity is N-type, and the second-polarity is P-type.

3. The semiconductor device according to claim **1**, wherein the substrate has the second-polarity.

4. The semiconductor device according to claim **1**, wherein the first isolation region comprises:
- a first doped ring structure formed in the substrate; and
- a first buried layer formed in the substrate and adjacent to the bottom of the first doped ring structure.

5. The semiconductor device according to claim **4**, wherein the first doped ring structure comprises:
- a first high voltage lightly-doped region; and
- a first well region formed in the first high voltage lightly-doped region and having a dopant concentration higher than that of the first high voltage lightly-doped region.

6. The semiconductor device according to claim **1**, further comprising:
- a second isolation region formed in the substrate and surrounding the first isolation region, wherein the second isolation region has the first-polarity.

7. The semiconductor device according to claim **6**, wherein the second isolation region comprises a connecting pin for receiving an individual voltage.

8. The semiconductor device according to claim **6**, wherein the second isolation region comprises:
- a second doped ring structure formed in the substrate; and
- a second buried layer formed in the substrate and adjacent to the bottom of the second doped ring structure.

9. The semiconductor device according to claim **8**, wherein the second doped ring structure comprises:
- a second high voltage lightly-doped region; and
- a second well region formed in the second high voltage lightly-doped region and having a dopant concentration higher than that of the second high voltage lightly-doped region.

10. The semiconductor device according to claim **9**, wherein the second doped ring structure further comprises: